R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

SUPPORT FOR CLAIM AMENDMENTS

Support for the amendments to the claims can be found in the drawings as originally filed, for example in FIGS. 2-7, and in the specification as originally filed, for example, on page 25, line 10 through page 33, line 11, on page 48, lines 9-20, and on page 49, line 18 through page 50, line 2. As such, no new matter has been introduced.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 1, 3-6, 12, 14, 15 and 17-21 under 35 U.S.C. §103 as being unpatentable over Piret et al. (U.S. Patent No. 4,486,882; hereafter Piret) in view of Hidaka et al. (U.S. Patent No. 4,730,320; hereinafter Hidaka) in further view of Chen (U.S. Patent No. 4,464,753) has been obviated by appropriate amendment and should be withdrawn.

The rejections of claims 2, 7-11, 13 and 16 under 35 U.S.C. §103 as being unpatentable over Piret, Hidaka and Chen in view of Stiffler (U.S. Patent No. 4,736,376) have been obviated by appropriate amendment and should be withdrawn.

The rejections of claims 22 and 23 under 35 U.S.C. §103 as being unpatentable over Hidaka in view of Chen in further view

of Stiffler have been obviated by appropriate amendment and should be withdrawn.

In contrast to the cited references, the presently claimed invention (claim 1) provides a detector circuit configured to (i) receive the second syndrome signal, (ii) detect an error when bits of the second syndrome signal are not all the same state and (iii) generate one or more single error signals when a single bit error is detected in the read data and the read parity signals, a double error signal when an error is detected in two bits of the read data and the read parity signals, and an error detected signal when either one of the one or more single error signals or the double error signal are asserted in response to the second syndrome signal. Claims 14 and 15 include similar limitations. Piret, Hidaka, Chen and Stiffler do not appear to teach or suggest a detector circuit configured to (i) receive the second syndrome signal, (ii) detect an error when bits of the second syndrome signal are not all the same state and (iii) generate one or more single error signals when a single bit error is detected in the read data and the read parity signals, a double error signal when an error is detected in two bits of the read data and the read parity signals, and an error detected signal when either one of the one or more single error signals or the double error signal are asserted in response to the second syndrome signal, as presently claimed. Therefore, Piret, Hidaka, Chen and Stiffler do not appear to teach or suggest each and every element of the presently claimed invention. As such, the presently claimed invention is fully

patentable over the cited reference and the rejection should be withdrawn.

Claims 2-13 and 16-21 depend, directly or indirectly, from either claim 1 or claim 15 which are now believed to be allowable. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Furthermore, Applicants' representative traverses the statement in the final Office Action that

> if all the syndromes are zero, then inherently there is no error and only the non-zero syndromes are necessary to generate error locations, hence the error location signal is generated in response to the non-zero syndromes, i.e., the error location signal is generated in response to fewer than all of said bits of said second syndrome signal when there exist non-zero syndromes (see page 6, lines 3-8 of the final Office Action mailed November 30, 2005),

Inherency requires certainty of results, not mere possibility. See, e.g., *Ethyl Molded Products Co. v. Betts Package, Inc.*, 9 U.S.P.Q. 2d 1001 (E.D.Ky 1988). The Office Action does not present objective evidence or a convincing line of reasoning that Hidaka generates an error location signal that necessarily uses fewer than all of the bits of a syndrome signal.

Furthermore, the rejections of claims 7 and 9 on the grounds of engineering design choice do not appear to be proper. The Office Action does not present objective evidence to support such a position. Furthermore, the reasons given for asserting engineering design choice, actual design requirements such as cost,

feasibility, available space, stray capacitance, available circuitry, design layout and intrinsic qualities of circuit components that affect overall efficiency and cost of circuitry (see page 13, lines 1-4 and 13-14 and page 15, lines 7-9 and 19-21 of the final Office Action mailed November 30, 2005), are too general because they could almost cover any alteration contemplated of the cited references and do not specifically address why the specific proposed modification would have been obvious. As such, the rejections do not appear to be proper and should be withdrawn.

With respect to claim 22, the cited references do not teach or suggest each and every element of the present pending claim 22. Specifically, claim 22 provides a syndrome encoder circuit configured to (i) receive a read data signal AND a read parity signal and (ii) generate a syndrome signal in response to the read data signal and the read parity signal, where the syndrome encoder circuit comprises a type of syndrome encoder selected from the group consisting of (i) non-inverting exclusive-OR gates with an output inverted by a NOT gate, (ii) inverting exclusive-OR gates, (iii) inverting exclusive-OR gates with an output inverted by a NOT gate, (iv) non-inverting exclusive-NOR gates, (v) non-inverting exclusive-NOR gates with an output inverted by a NOT gate, (vi) inverting exclusive-NOR gates, and (vii) inverting exclusive-NOR gates with an output inverted by a NOT gate.

The position taken in the Office Action (see pages 2 and 10 of the final Office Action mailed November 30, 2005 and page 11, line 20 through page 12, line 6 of the non-final Office Action

dated April 29, 2005) that "Figure 7 in Stiffler teaches first syndrome signal [c1...c4] is produced using non-inverting exclusive-OR gates and non-inverting exclusive-OR gates with an output inverted by a NOT gate is not technically correct. In particular, Stiffler does not support the interpretation presented in the Office Action. Specifically, Stiffler states that the signals [b1...b16] received by the circuit shown in FIG. 7 of Stiffler are bits of a data word (see column 8, lines 22-37 of Stiffler). The circuit in FIG. 7 of Stiffler does not receive a parity signal. Furthermore, Stiffler explicitly provides that the signals [c1...c4], which are generated by the circuit shown in FIG. 7 of Stiffler, are computed parity relationships which are used with nyble parity signals [g1...g4] **to generate syndrome bits.** Stiffler states:

> **Each circuit half combines the results of the four parity relationships computed from the data bits available to it with the four nyble parities computed by the other half circuit to generate four syndrome bits** (half of the total eight-bit syndrome). This combination is performed in second stage syndrome generators 442 and 444. Generator 442 receives **four bits, c1-c4, corresponding to the four computed parity relationships calculated from the input data bits** via bus 438 and **four nyble parities, g1-g4**, received from the other circuit half over terminal 441 and bus 440. Similarly generator 444 receives the complemented parity relationship bits, e1-e4, from generator 430 over bus 437 and the nyble parity bits g1-g4 from the other decoder half. Generator 442 generates four syndrome bits, h1-h4, on bus 456 and generator 444 generates four bits, i1-i4, which are the complements of the bits generated by generator 442. The complemented bits are provided on bus 454 to be used in a

later stage of processing (column 8, line 63-column 9, line 13 of Stiffler, emphasis added).

Since "one of ordinary skill in the art at the time the invention was made would have known that syndromes are equal to the difference between received parity and newly generated parity at the receiver" (see Examiner's admission in last five lines on page 2 of the final Office Action dated November 30, 2005) and (i) the circuit shown in FIG. 7 of Stiffler receives only data bits (i.e., the signals b1...b16) and (ii) the signals [c1...c4] are computed parity relationships rather than a syndrome signal, it follows that one of ordinary skill in the art at the time the invention was made would not view FIG. 7 of Stiffler as teaching or suggesting **a syndrome encoder circuit configured to (i) receive a read data signal AND a read parity signal and (ii) generate a syndrome signal in response to the read data signal AND the read parity signal**, wherein said syndrome encoder circuit comprises a type of syndrome encoder selected from the group consisting of (i) non-inverting exclusive-OR gates with an output inverted by a NOT gate, (ii) inverting exclusive-OR gates, (iii) inverting exclusive-OR gates with an output inverted by a NOT gate, (iv) non-inverting exclusive-NOR gates, (v) non-inverting exclusive-NOR gates with an output inverted by a NOT gate, (vi) inverting exclusive-NOR gates, and (vii) inverting exclusive-NOR gates with an output inverted by a NOT gate, as presently claimed. Furthermore, the Office Action admits that the step of generating parity is only part of the step

of generating a syndrome (see Examiner's admission in last five lines on page 2 of the final Office Action dated November 30, 2005). Therefore, the Office Action does not meet the Office's burden to factually establish that the combination of Hidaka, Chen and Stiffler teach or suggest each and every element of the presently claimed invention. As such, the presently claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Claim 23 depends directly from claim 22 which is believed to be allowable. As such, the presently claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

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